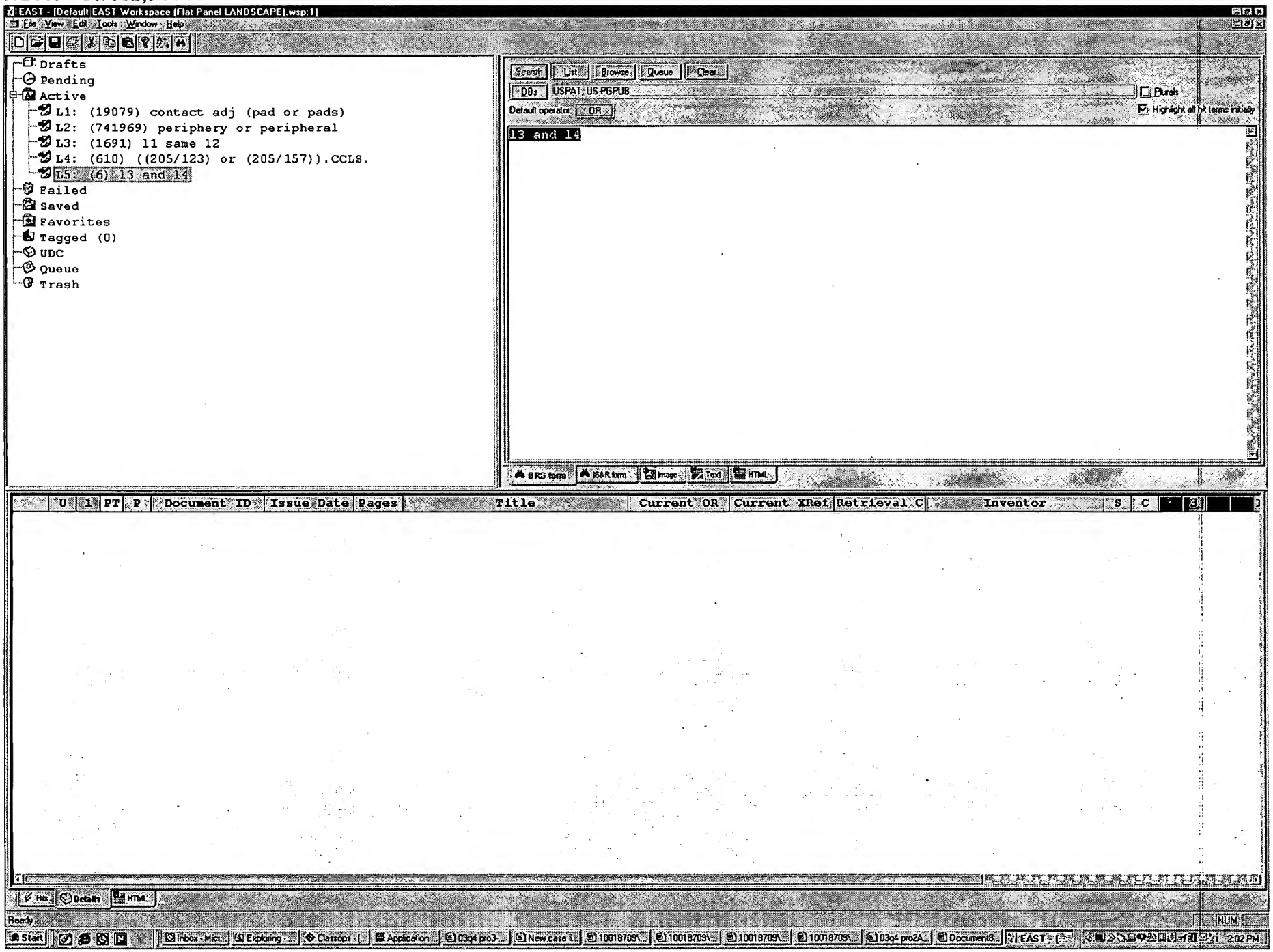
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EAST Browser - L5: (6) 3 and 4 | US 6187164 B1 | Tag: S | Doc: 2/6 (SORTED) | Format : KWIC

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2	US 6187164 B1	13							☑				USPAT
3	US 4205099 A	6						☑					USPAT
4	US 20030168346 A1	46						☑					US-PGPU
5	US 20030094374 A1	7						☑					US-PGPU
6	US 20020029961 A1	42						☑					US-PGPU

US-PAT-NO: 6187164

DOCUMENT-IDENTIFIER: US 6187164 B1
See image for Certificate of Correction

TITLE: Method for creating and testing a combinatorial array employing individually addressable electrodes

---------- KWIC ---------

Detailed Description Text - DETX (3):
The individually addressable electrode arrays 10 of the present invention are illustrated in FIGS. 1A and 1B. The arrays 10 consist of either sixty-four or sixty-six independent electrodes 12 (with areas of between 1 and 2 mm.sup.2) that are fabricated on inert substrates 14. Arrays with as little as 10 or as many as 100 electrodes may be made in accordance with the methods provided in the present invention. Example substrates include, but are not limited to, glass, quartz, sapphire, alumina, plastics, or thermally treated silicon. Other suitable substrate materials will be readily apparent to those of skill in the art. The individual electrodes 12 are located substantially in the center of the substrate 14, and are connected to contact pads 13 around the periphery of the substrate with wires 16. The electrodes 12, associated wires 16, and contact pads 13 are fabricated from conducting materials (such as gold, silver, platinum, copper, or other commonly used electrode materials). In a preferred embodiment of the present invention, the arrays are fabricated on standard 3" thermally oxidized single crystal silicon wafers, and the electrodes are gold with surface areas of about 1.26 mm.sup.2.

Detailed Description Text - DETX (4):
Still referring to FIGS. 1A and 1B, a patterned insulating layer 18 covers the wires 16 and an inner portion of the peripheral contact pads 13, but leaves the electrodes and the outer portion of the peripheral contact pads exposed (preferably approximately half of the contract pad is covered with this insulating layer). Because of the insulating layer 18, it is possible to connect a lead (e.g., an alligator clip) to the outer portion of a given contact pad and address its associated electrode while the array is immersed in solution, without having to worry about reactions that can occur on the wires or peripheral contact pads. The insulating layer may be, for example, glass, silica (SiO.sub.2), alumina (Al.sub.2 O.sub.3), magnesium oxide (MgO), silicon nitride (Si.sub.3 N.sub.4), boron nitride (BN), yttrium oxide (Y.sub.2 O.sub.3), titanium dioxide (TiO.sub.2), hardened photoresist, or other suitable material known to be insulating in nature.

Detailed Description Text - DETX (13):
Referring to FIG. 4C, an exploded view of the components of the anode assembly is shown. The glass housing 82 of the cell is fit over the inner flange 106 of a molded adapter 102 and is held in place against the adapter with an o-ring 100. This o-ring provides a water-tight seal for this part of the assembly. The diameter of the outer flange 104 of the adapter 102 is the same as that of the glass housing, while that of the inner flange 106 is slightly smaller allowing one half of it to fit into the glass housing and the other half of it to fit into the remaining pieces of the anode assembly. A groove 108 is cut into the lower lip of the adapter 102. This groove holds an

(12) **United States Patent**
Warren et al.

(10) **Patent No.: US 6,187,164 B1**
(45) **Date of Patent: Feb. 13, 2001**

(54) **METHOD FOR CREATING AND TESTING A COMBINATORIAL ARRAY EMPLOYING INDIVIDUALLY ADDRESSABLE ELECTRODES**

(75) Inventors: **Christopher J. Warren**, Mountain View; **Robert C. Haushalter**, Los Gatos; **Leonid Matsiev**, Cupertino, all of CA (US)

(73) Assignee: **Symyx Technologies, Inc.**, Santa Clara, CA (US)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/119,187**

(22) Filed: **Jul. 20, 1998**

Related U.S. Application Data

(63) Continuation-in-part of application No. 08/941,170, filed on Sep. 30, 1997.

(51) **Int. Cl.**[7] **C25D 5/02; C25D 21/12**

(52) **U.S. Cl.** **205/81; 205/118; 205/122; 205/123; 205/136; 205/775; 205/782**

(58) **Field of Search** 205/122, 118, 205/123, 228, 81, 136, 775, 782; 204/224, 230.7, 230.1

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Chu, Deryn, et al. *J. Electrochem. Soc.*, vol. 143, No. 5, pp. 1685–1690, (1996). Month of publication not available.

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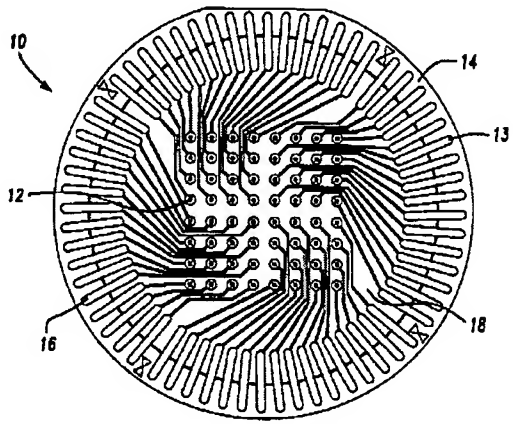
Primary Examiner—Kathryn Gorgos
Assistant Examiner—William T. Leader
(74) *Attorney, Agent, or Firm*—Dobrusin Darden; Thennisch & Lorenz PLLC

(57) **ABSTRACT**

An electrochemical deposition and testing system consisting of individually addressable electrode arrays, a fully automated deposition head, and a parallel screening apparatus is described. The system is capable of synthesizing and screening millions of new compositions at an unprecedented rate.

16 Claims, 6 Drawing Sheets



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5	US 20030094374 A	7											US-PGPU
6	US 20020029961 A	42											US-PGPU

US-PAT-NO: 4205099

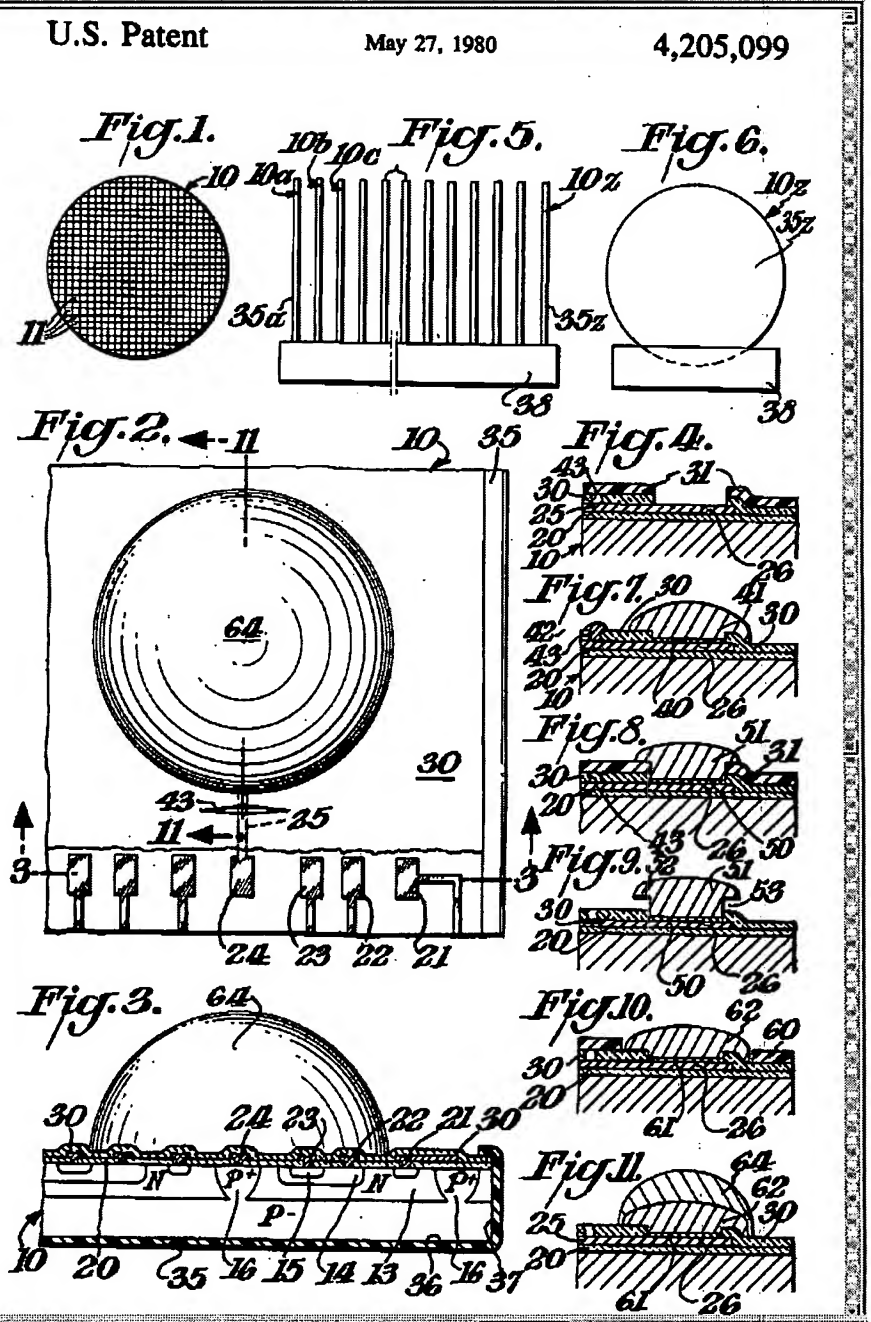
DOCUMENT-IDENTIFIER: US 4205099 A

TITLE: Method for making terminal bumps on semiconductor wafers

---------- KWIC ---------

Drawing Description Text - DRTX (3):
FIG. 2 shows in magnified detail a portion of one of the devices of FIG. 1 located near the periphery of the wafer. A portion of the overlying quartz layer is broken away in an area over the contact pads.

Current US Cross Reference Classification - CCXR (1):
205/123



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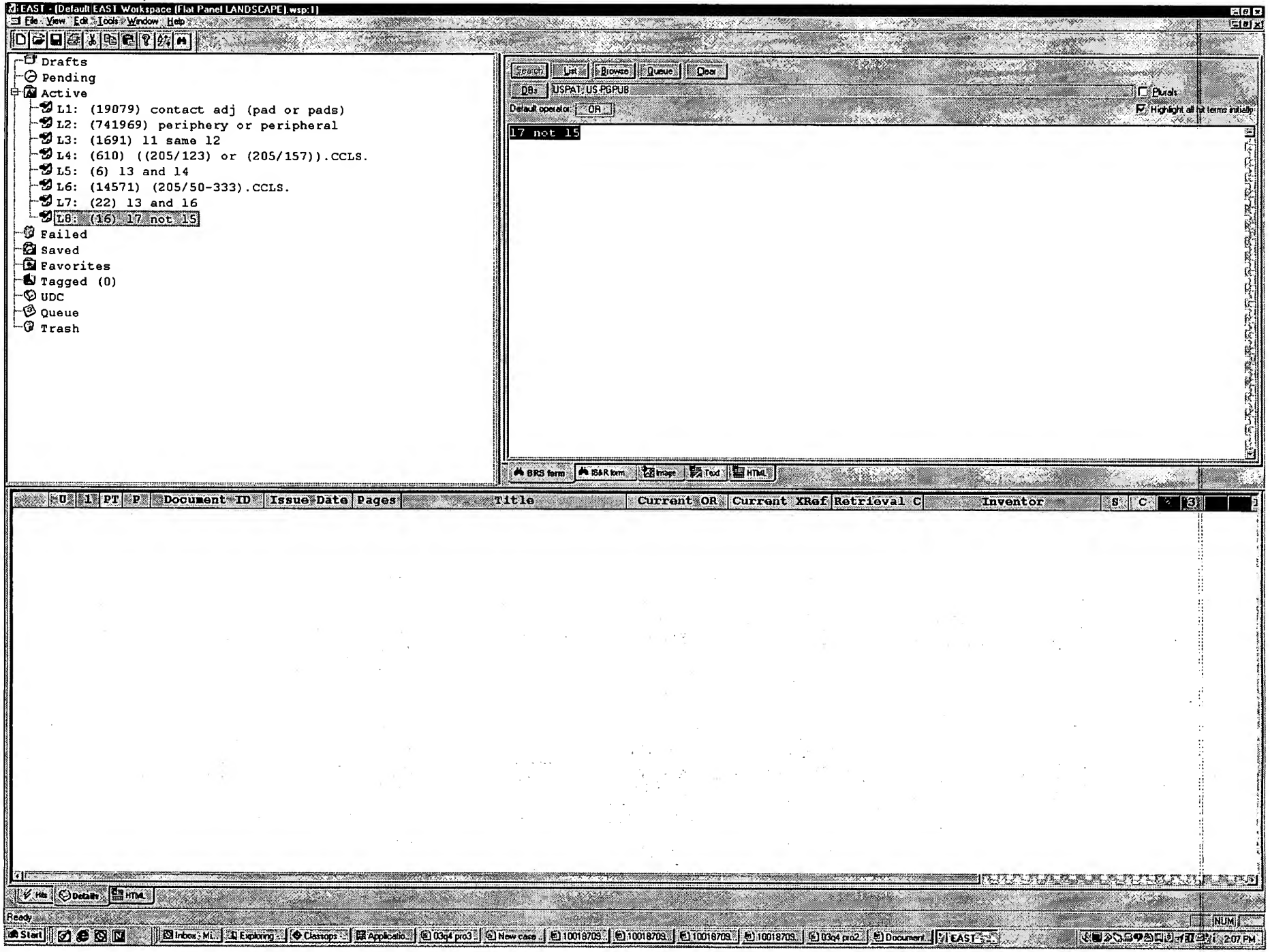
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L5: (6) l3 and l4
L6: (14571) (205/50-333).CCLS.
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3	US 6582578 B1	54			☑				USPAT
4	US 6576110 B2	35			☑				USPAT
5	US 6551484 B2	46			☑				USPAT
6	US 6416647 B1	28			☑				USPAT
7	US 6241868 B1	9			☑				USPAT

US-PAT-NO: 6241868

DOCUMENT-IDENTIFIER: US 6241868 B1

TITLE: Method for electroplating a film onto a substrate

---------- KWIC ---------

Claims Text - CLTX (2):
a) providing a substrate with a top side including a plating surface having a plurality of plating seeds, an underside having a plurality of contact pads, and a peripheral edge, wherein said plating seeds are electrically connected to said plurality of contact pads;

Current US Original Classification - CCOR (1):
205/118

(12) **United States Patent**
Biggs et al.

(10) **Patent No.: US 6,241,868 B1**
(45) **Date of Patent: Jun. 5, 2001**

(54) **METHOD FOR ELECTROPLATING A FILM ONTO A SUBSTRATE**

(75) Inventors: **Glen N. Biggs**; **Donald M. Brewer**, both of Wappingers Falls; **James E. Fluegel**, Tivoli; **Suryanarayana Kaja**, Hopewell Junction; **Ashwani K. Malhotra**, Newburgh; **Phillip W. Palmatier**, Hopewell Junction, all of NY (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/541,018**

(22) Filed: **Mar. 31, 2000**

Related U.S. Application Data

(62) Division of application No. 09/181,129, filed on Oct. 28, 1998, now Pat. No. 6,077,405.

(51) Int. Cl.[7] **C25D 5/02**
(52) U.S. Cl. **205/118**
(58) Field of Search 205/118

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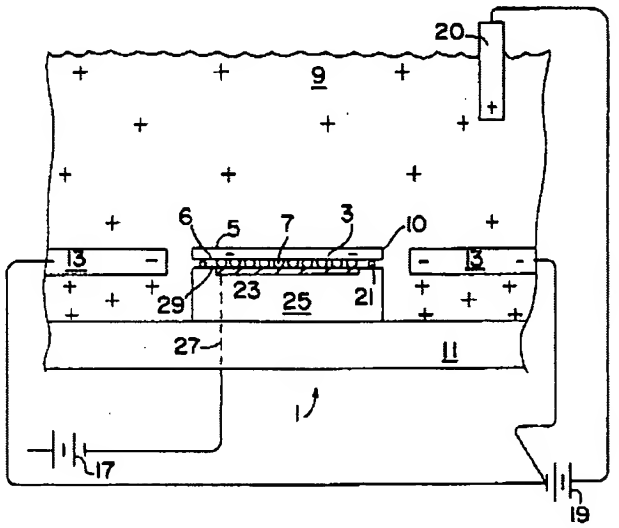
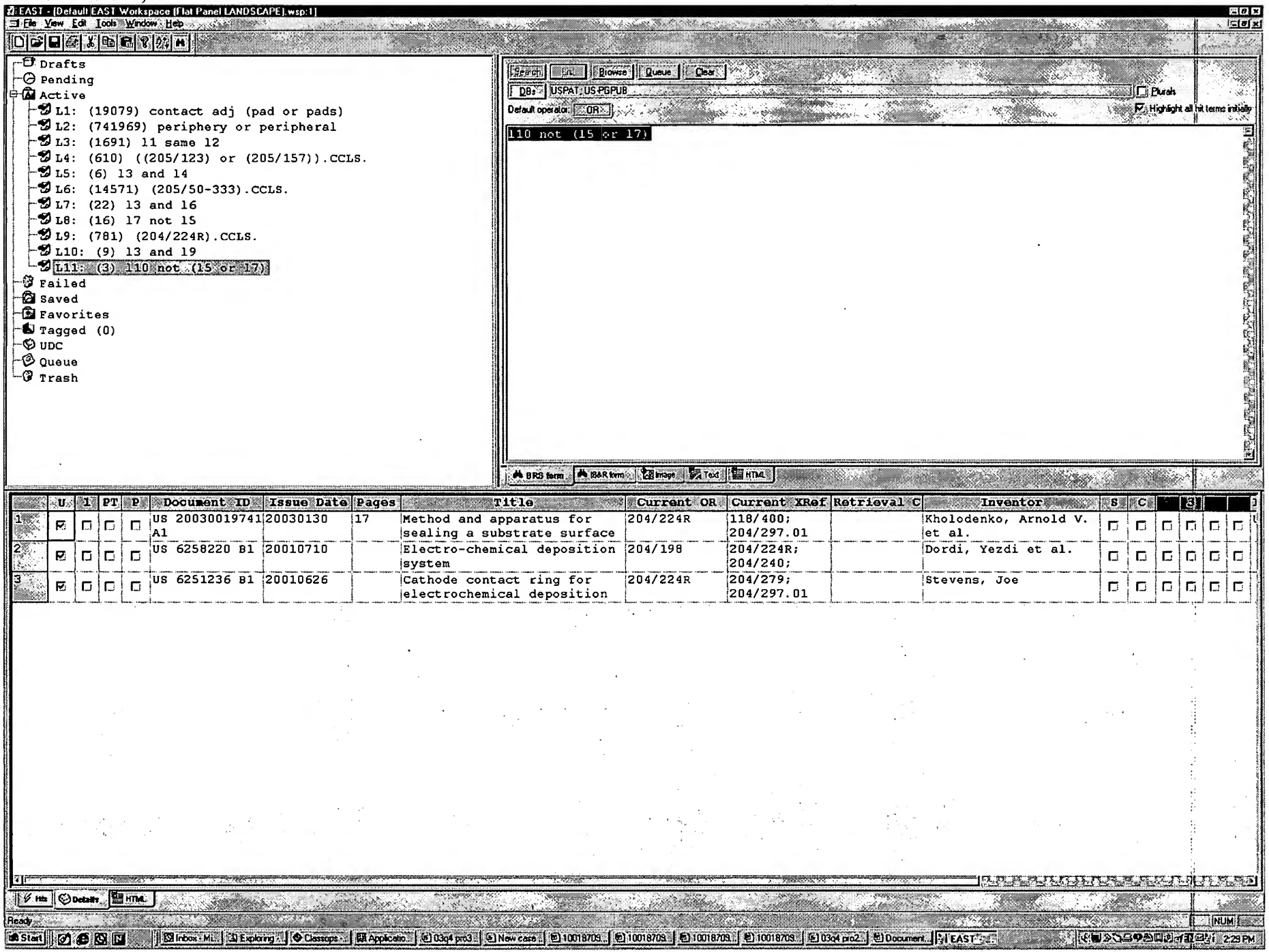
Primary Examiner—Kathryn Gorgos
Assistant Examiner—Erica Smith-Hicks
(74) *Attorney, Agent, or Firm*—Ratner & Prestia; Ira D. Blecker, Esquire

(57) **ABSTRACT**

A method for electroplating a film onto a substrate. Electrical power is supplied to the plating surface through electrical contact made to contact pads on the underside of the substrate. Contact to the contact pads is made within a liquid-tight region. The contact pads are connected to the plating surface through the substrate. Because the contact scheme is provided within a liquid-tight region on the underside of the substrate, the contacts do not erode or become plated, nor do they consume an area of the plating surface.

14 Claims, 4 Drawing Sheets

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2 US 6258220 B1 20010710 Electro-chemical deposition system 204/198 204/224R; 204/240; Dordi, Yezdi et al.
3 US 6251236 B1 20010626 Cathode contact ring for electrochemical deposition 204/224R 204/279; 204/297.01 Stevens, Joe
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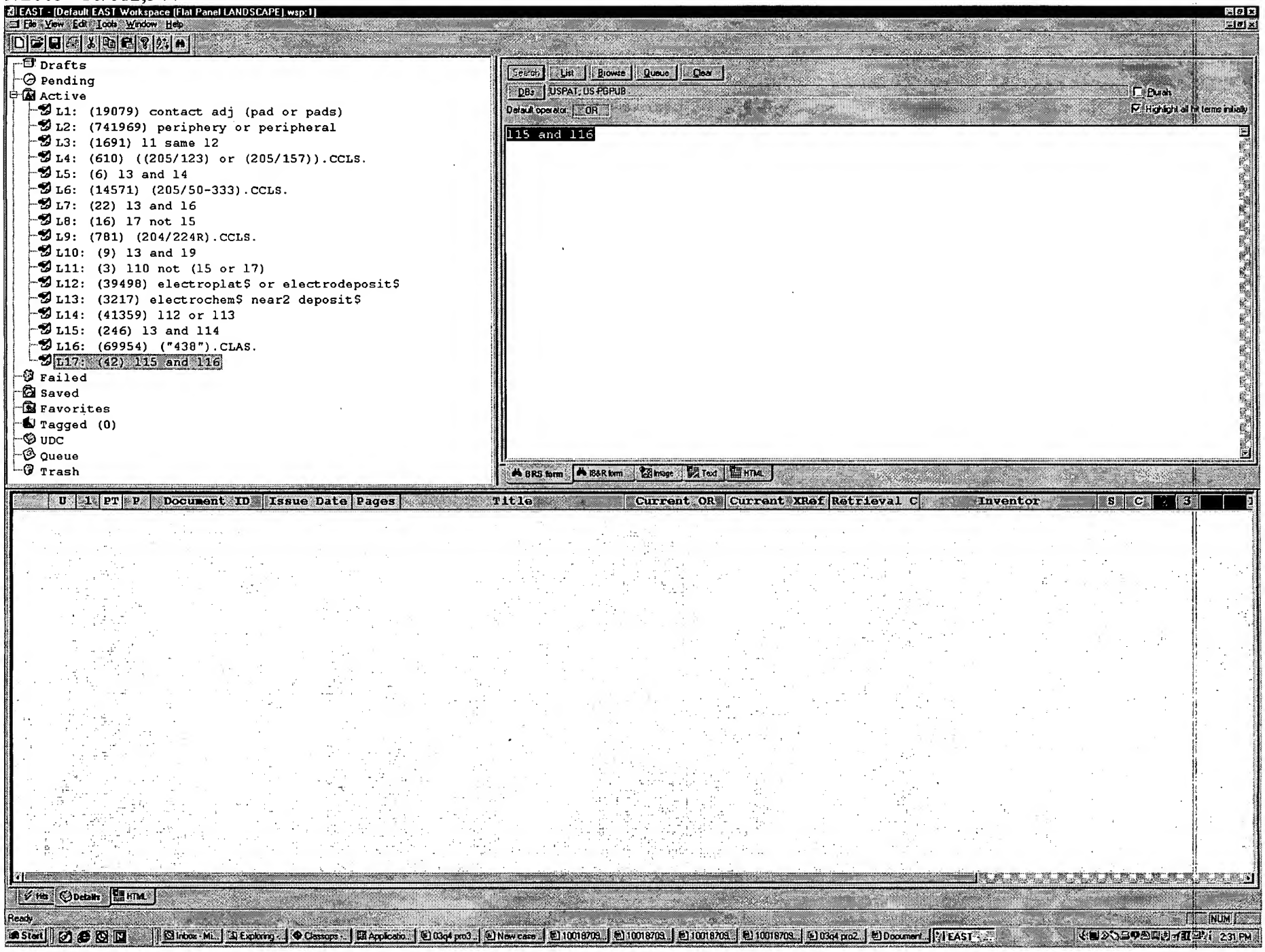
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4	US 6548393 B1	28				☑					USPAT
5	US 6537831 B1	18				☑					USPAT
6	US 6506672 B1	19				☑					USPAT
7	US 6499216 B1	19				☑					USPAT

US-PAT-NO: 6596624

DOCUMENT-IDENTIFIER: US 6596624 B1

TITLE: Process for making low dielectric constant hollow chip structures by removing sacrificial dielectric material after the chip is joined to a chip carrier

---------- KWIC ---------

Brief Summary Text - BSTX (11):

An article on pp. 575-585 published in the IBM Journal of Research and Development Volume 42 No. 5, September 1998, "Electrochemical process for advanced package fabrication", coauthored by S. Krongelb, J. A. Tornello and L. T. Romankiw, the latter of whom is the inventor herein, includes a description of a process of making, and certain performance measurements of, a multilevel structure which incorporates polyimide dielectric layers and is on a chip carrier. In preparation for creating the scanning electron micrograph (SEM) images of the structure, seen as FIGS. 3 and 4 on p. 580 and FIG. 5 on p. 581, polyimide was removed from a region of the structure by ashing in an oxygen containing plasma. Electrical measurements were performed in order to ascertain that the metallurgy was sound and that good metal-to-metal contact had been obtained during electroplating. The present invention, in which solid dielectric material is replaced by air or vacuum in order to obtain a mechanically sound, multilevel final structure having minimal Er, was not foretold by the reference. Up to the time of the present invention it was assumed that dielectric such as polyimide would provide an minimum Er which would be adequate for the thin film package (chip carrier).

Brief Summary Text - BSTX (15):

In an article "Future interconnect technologies and copper metallization" pages 63, 64, 68, 72, 74, 76 and 79 of the October, 1998 issue of the journal Solid State Technology, authors X, W. Lin and Dipu Pramanik describe a movement to electroplated copper wiring from aluminum wiring in the ICs of the future as an inevitable necessity. The authors further identify physical vapor deposited (PVD) or chemical vapor deposited (CVD) Ta, TaN, Si3N4 or W as known barriers to copper diffusion into silicon. Plated Cu is used in the present invention, in conjunction with diffusion barriers.

Detailed Description Text - DETX (7):

The silicon substrate (5) of a structure of the present invention for BEOL application is shown in FIG. 1A. An interdiffusion barrier followed by seed (neither shown) have been deposited and conductive copper wiring patterned onto the substrate (5). Support studs (7) around the periphery of the chip provide additional support as well as heat dissipation. The additional supports are preferably made of the same material as the wiring (6) and the conductive vias (9), preferably copper, and deposited by plating. Vias (9) are used as conductors between wiring levels and as support studs. Conductive vias join a number of wiring levels and ultimately terminate at contact pads (4).

Detailed Description Text - DETX (30):

7. A seed layer is sputtered, resist is applied, exposed and developed and

(12) **United States Patent**
Romankiw

(10) **Patent No.: US 6,596,624 B1**
(45) **Date of Patent: Jul. 22, 2003**

(54) **PROCESS FOR MAKING LOW DIELECTRIC CONSTANT HOLLOW CHIP STRUCTURES BY REMOVING SACRIFICIAL DIELECTRIC MATERIAL AFTER THE CHIP IS JOINED TO A CHIP CARRIER**

(75) Inventor: **Lubomyr Taras Romankiw**, Briarcliff Manor, NY (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 75 days.

(21) Appl. No.: **09/619,745**

(22) Filed: **Jul. 19, 2000**

Related U.S. Application Data

(60) Provisional application No. 60/146,772, filed on Jul. 31, 1999.

(51) **Int. Cl.**[7] **H01L 21/4763**

(52) **U.S. Cl.** **438/619**; 438/623; 438/633

(58) **Field of Search** 438/619, 622, 438/623, 631, 633, 113

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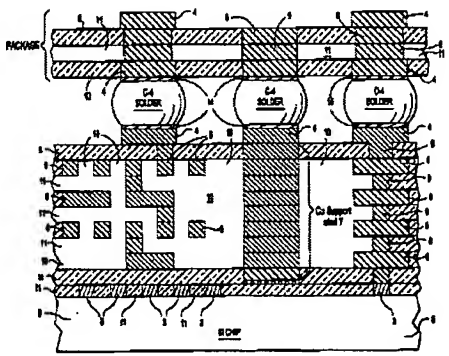
(List continued on next page.)

Primary Examiner—Carl Whitehead, Jr.
Assistant Examiner—Stephen V. Smoot
(74) *Attorney, Agent, or Firm*—Judith D. Olsen; Robert Trepp

(57) **ABSTRACT**

Disclosed is a multilayer integrated circuit structure joined to a chip carrier, and a process of making, in which the area normally occupied by a solid dielectric material in the IC is at least partially hollow. The hollow area can be filled with a gas, such as air, or placed under vacuum, minimizing the dielectric constant. Several embodiments and processing variants are disclosed. In one embodiment of the invention, the wiring layers, which are embedded in a temporary dielectric, alternate with via layers, also embedded in a temporary dielectric, in which the vias, besides establishing electrical communication between the wiring layers, also provide mechanical support for after the temporary dielectric is removed. Additional support is optionally provided by support structures though the interior levels and at the periphery of the chip. The temporary dielectric is removed subsequent to joining by dissolution or by ashing in an oxygen-containing plasma.

24 Claims, 6 Drawing Sheets



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6	US 6506672 B1	19							☑				USPAT
7	US 6499216 B1	19							☑				USPAT
8	US 6492252 B1	59							☑				USPAT
9	US 6483330 B1	18							☑				USPAT
10	US 6388322 B1	14							☑				USPAT
11	US 6350668 B1	19							☑				USPAT

US-PAT-NO: 6350668

DOCUMENT-IDENTIFIER: US 6350668 B1

TITLE: Low cost chip size package and method of fabricating the same

---------- KWIC ---------

Drawing Description Text - DRTX (26):
FIGS. 10a to 10h refers to the third preferred embodiment FIG. 10a shows a wafer 301 and a chip 302 with peripheral chip contact pads 304.

Detailed Description Text - DETX (4):
FIG. 2 is a top plan view of a wafer 301 which contains numerous integrated circuit (IC) chips 302. Adjacent chips are separated by borders 303 referred to as scribe lines. In the present embodiment, each IC chip contains the complete integrated circuit elements. At the top layer, the chip contains regions called contact pads whereby connections for the input and output signals from the chip can be made. As shown in FIG. 3, these input and output contact pad regions, referred to as chip contact pads, are usually distributed in a ring like structure along the periphery of the chip and are illustrated as 304. An integrated circuit (IC) contains a large number of devices which are derived from transistors. In order to provide more functionality from the chip, a larger number of such devices need to be incorporated. This is referred to as increasing the integration level of the integrated circuit. As the integration level of the IC chip increases so does the number of required I/O connections in accordance with relationship called Moore's law. Thus, a larger number of chip contact pads need to be accommodated along the periphery of the chip. Increasing the size of the chip in order to accommodate these large number of chip contact pads is not economically viable due to the fact that processed silicon area is very expensive. Thus, the trend has been towards decreasing the size as well as separation of the connection pads. However, closely spaced and small contact pads are difficult to connect to the external world. Therefore, approaches have been developed for redistributing these I/O pads on the entire surface of the chip by using redistribution layers. One embodiment of the present invention uses this general approach in a novel way.

Detailed Description Text - DETX (10):
Deposition of the metal bumps 311-1 can be done by several established techniques. These include electro and electroless plating, evaporation using a metal shadow mask, or printing of a metal paste through a stencil aperture. Alternatively, a wire bonder can be used for bonding metal studs via a process referred to as "wire bonder stud bumping", wherein the wire bonder is used to deposit a gold or solder stud bump. A detailed description of this process is contained in "Ball Bumping and Coining Operations for TAB and Flip Chip" by Lee Levine, Proc. Electronics Components and Technology Conference, 1997, pp 265-267 and references therein, which is incorporated herein by reference. Examples of bump materials are 90/10 Pb/Sn solder, 63/37 Pb/Sn eutectic, and electrolessly plated nickel. For electroplated solder bumps, UBM layer 310 could be configured from a combination of Cr and Cu layers. The Cr layer functions as an adhesion or glue layer whereas the Cu layer provides a

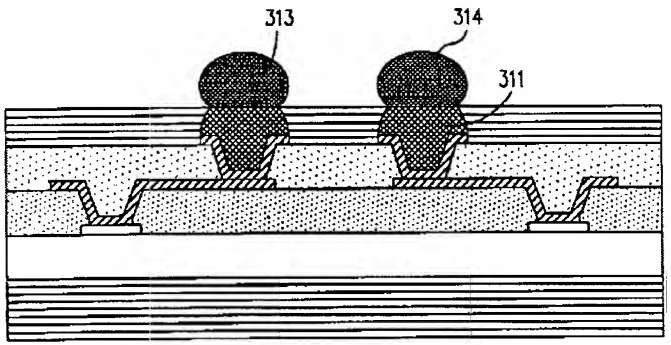

FIG. 8d

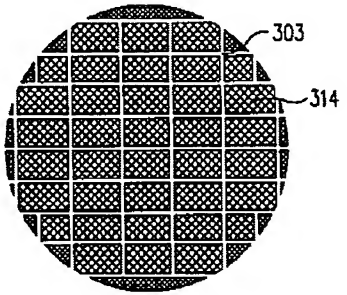

FIG. 8e

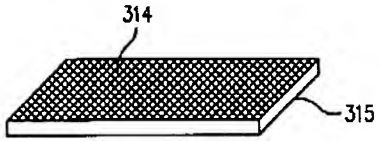

FIG. 8f

EAST Browser - L17: [42] 15 and 16 | US 6316289 B1 | Tag: S | Doc: 13/42 (SORTED) | Format : KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	U	S	C	P	Kind Codes	Sou
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8	US 6492252 B1	59									USPAT
9	US 6483330 B1	18									USPAT
10	US 6388322 B1	14									USPAT
11	US 6350668 B1	19									USPAT
12	US 6329606 B1	11									USPAT
13	US 6316289 B1	17									USPAT

US-PAT-NO: 6316289

DOCUMENT-IDENTIFIER: US 6316289 B1

TITLE: Method of forming fine-pitch interconnections employing a standoff mask

---------- KWIC ---------

Detailed Description Text - DETX (10):

The most precise openings and the finest features may be achieved by a third method known as electroforming. In this technique, the same photo-resist materials that are used in conventional semiconductor wafer processing are used to form the fine openings and features, and electroplating or electroforming or electro-depositing is used to build up a thin metal foil. Precision openings having a dimension as fine as 2.5 microns have been fabricated by electroforming. Other methods, such as screen emulsion and die cutting, may also be employed. Combinations of two or three of the foregoing techniques may be employed for better cost effectiveness, such as where both fine and larger openings and features are to be formed in the same metal membrane.

Detailed Description Text - DETX (26):

Then, a pattern of stencil openings 214, 216, 218 corresponding to the pattern, for example, of contact pads on the semiconductor wafer with which standoff stencil 200 is to be utilized, is etched through the 2-mil thick portion of stainless steel sheet 202 from the second side thereof to cavities 204, 204'. The features of standoff layer 212, 212a, 212b, 212c are laterally spaced away from stencil openings 214, 216, 218. A first exemplary pattern of stencil openings 214, 216 corresponding to contact pads of a first device on the semiconductor wafer which are in four rows around the periphery thereof, has two outer peripheral rows of 3-mil diameter openings 214 at a 6-mil pitch for depositing 3-mil diameter, 4-mil high bumps of conductive material on the semiconductor wafer and has two inner peripheral rows of 2-mil diameter openings 216 at a 4-mil pitch for depositing 2-mil diameter, 4-mil high bumps of conductive material on the semiconductor wafer. Standoff features 212 and 212a of standoff layer 212, 212a, 212b, 212c form a laterally spaced away peripheral standoff feature around the pattern of openings 214, 216, but it is not necessary that a standoff feature completely surround any pattern of openings. A standoff feature 212c is located in a central region of the pattern of openings 214, 216, as is convenient where the pattern of openings 214, 216 is a peripheral pattern, to support that portion of standoff stencil 200 during deposition, as is generally desirable where the pattern of holes is larger and the stencil is thinner.

Detailed Description Text - DETX (27):

Second and third exemplary patterns of openings 218 corresponding, for example, to contact pads of second and third devices on the semiconductor wafer, may be in different or like patterns. A second pattern of openings 218 are shown as being in one row around the periphery of a device, and a second pattern of openings 218 are shown as being in a rectangular array. In any case, openings 218 may be of like diameter and/or pitch or of mixed diameter and/or pitch, and may be of the same or different diameter and/or pitch as openings 214, 216, but are also for depositing 4-mil high bumps of conductive

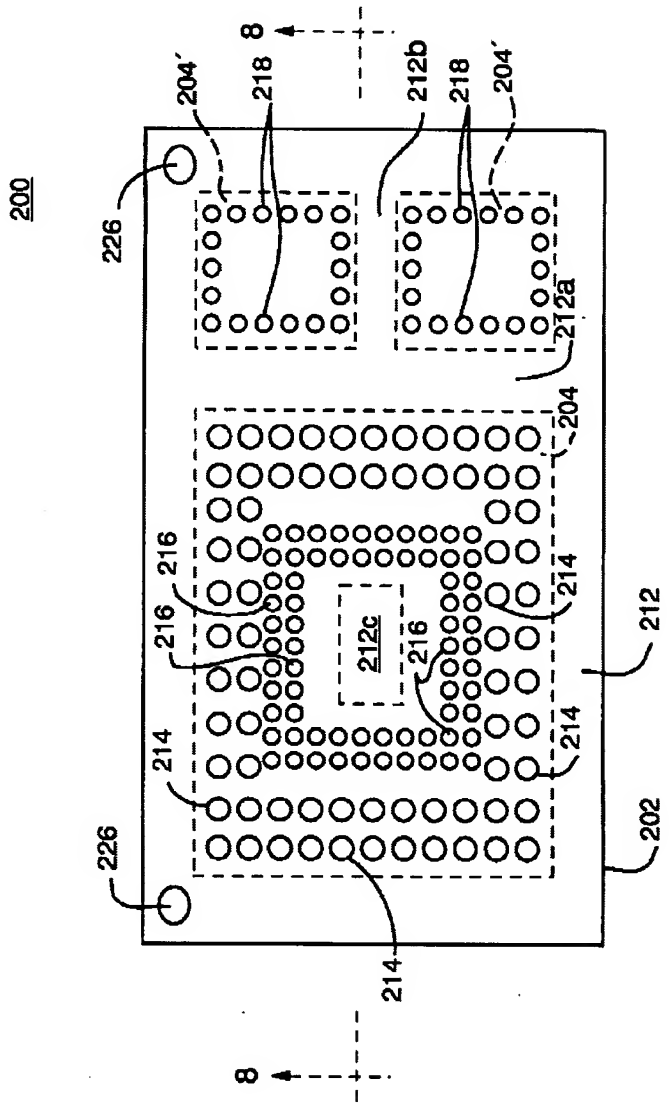

FIG. 7

EAST Browser - L17: (42) 15 and 16 | US 5966593 A | Tag: S | Doc: 23/42 (SORTED) | Format : KWIC

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#	Document ID	Pages	1	3	U	S	C	P	Kind Codes	Sou
17	US 6181569 B1	19								USPAT
18	US 6117694 A	24								USPAT
19	US 6046060 A	37								USPAT
20	US 6020220 A	10								USPAT
21	US 6017696 A	57								USPAT
22	US 6012224 A	13								USPAT
23	US 5966593 A	38								USPAT

US-PAT-NO: 5966593

DOCUMENT-IDENTIFIER: US 5966593 A

TITLE: Method of forming a wafer level contact sheet having a permanent z-axis material

---------- KWIC ---------

Detailed Description Text - DETX (7):
The first terminals 13 are grouped in the center of the base unit 7, above the wafer 1 having a corresponding pattern to the pattern of contact pads of the chips 2 on the wafer 1. The second terminals 14 are also on the lower surface 12 of the base unit 7, and are grouped outside of the periphery of the first terminals 13. The second terminals 14 may form a ring around the first terminals 13, may be grouped substantially on one side of the first terminals, or may be distributed over the entire lower surface 12 of the base unit 7 outside of the grouping of the first terminals 13. The second terminals 14 are connectable to the test signal generator 10 at contacts.

Detailed Description Text - DETX (170):
As a result, a blind via 72 is formed. Thereafter the inside of the well or via 72 is coated with a conductive metal 73, such as copper. Copper may be deposited by any suitable technique, such as, electroless plating, sputtering, evaporation, or deposition of a conductive coating which allows direct electrodeposition.

Detailed Description Text - DETX (177):
Suitable processes for forming the metal coating on the via include, but are not limited to a conventional electroless copper plating operation, sputtering, evaporation, or deposition of a conductive coating which allows direct electrodeposition, or any other suitable process. Additional electrolytically deposited copper may be added to thicken this deposit, thereby providing a more robust surface for additional process steps.

Current US Class - CLAS (3):
438

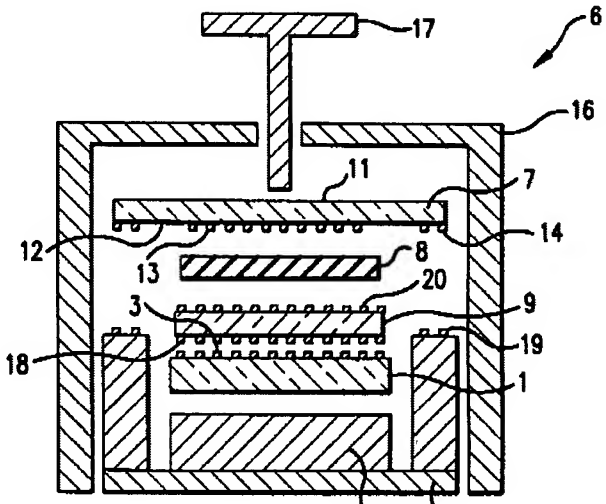

FIG.2

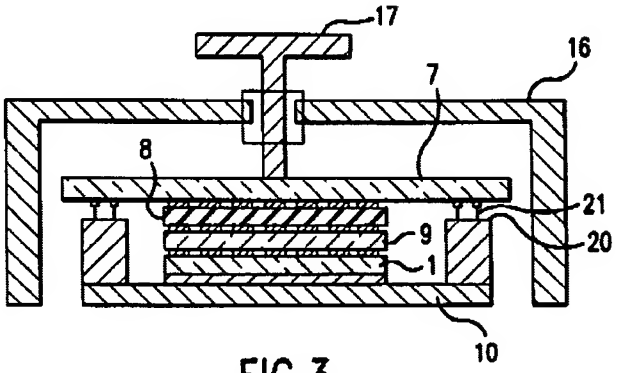

FIG.3

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20	US 6020220 A	10											USPAT
21	US 6017696 A	57											USPAT
22	US 6012224 A	13											USPAT
23	US 5966593 A	38											USPAT
24	US 5953594 A	16											USPAT
25	US 5907785 A	9											USPAT

US-PAT-NO: 5907785

DOCUMENT-IDENTIFIER: US 5907785 A

TITLE: Wafer with elevated contact substructures

---------- KWIC ----------

Brief Summary Text - BSTX (4):

There are a number of methods by which integrated circuit chips may be mounted on a higher level of assembly, such as a printed circuit board. For example, one such technique generally known as "A-wire" or "lead on chip" (LOC) involves placing the chip inside a plastic package and coupling certain contact points on the chip with somewhat rigid conductive leads by means of a thin wire bond. The leads are then bonded to corresponding contact pads on a printed circuit board, which thereby enables the chip to communicate with the board. In an alternative packaging scheme, generally referred to as "tape automated bonding" (TAB) the chip is mounted on a tape which is configured to also have a series of conductive leads, albeit somewhat flexible ones, which are used to make contact with conductive points around the periphery of the chip. The end of the lead opposite to the connection with the chip is then used to make contact with the higher level of assembly, which again may be a printed circuit board. In both LOC and TAB the leads establish the electrical paths by which the chip is accessed for signal transmission, as well as for providing power and ground.

Brief Summary Text - BSTX (5):

With regard to LOC and TAB, both such techniques generally require the higher level of assembly, such as a printed circuit board, to have a place for mounting the chip package which is larger than the chip itself. Since in both instances the chip, either by itself or when surrounded by a plastic package, will have the leads extend out from its periphery, the finished chip package will make a so-called "footprint" on the higher level of assembly that is necessarily larger than the chip itself. A further limitation of the TAB method of packaging in particular, is that TAB has been used for making connection with chip contact pads that are positioned around the periperhy of the chip, but not contact pads disposed in the central region of the chip. Many modern chips are now designed with their contact points in the center, as that particular arrangement tends to reduce the noise which may effect the operation of the electrical circuits contained within. TAB, therefore, is not well suited for use with chips configured with their contact points centrally located.

Detailed Description Text - DETX (15):

After the formation of bump 32, wafer 20 is next coated with a blanket deposit of a thin conductor, which is then patterned in accordance with the form of the permanent conductors 26. Then the wafer is electroplated with copper, the resist is stripped, and an etch step is performed to expose the thin conductor. The resulting structure is shown in FIG. 4D, from which it will be seen that conductors 26 (including conductors 26a and 26b) have been formed over the surface of insulator coating 42 and bump 32, and surface conductor 44 is deposited in via 30 in contact with via contact 40.

United States Patent [19]

Palagonia

[11] **Patent Number: 5,907,785**

[45] **Date of Patent: May 25, 1999**

[54] **WAFER WITH ELEVATED CONTACT SUBSTRUCTURES**

[75] Inventor: **Anthony Michael Palagonia**, Underhill, Vt.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **08/826,362**

[22] Filed: **Mar. 26, 1997**

Related U.S. Application Data

[62] Division of application No. 08/518,740, Aug. 24, 1995, Pat. No. 5,874,762.

[51] Int. Cl.[6] **H01L 21/44**

[52] U.S. Cl. **438/613**; 438/612; 438/615; 438/118

[58] Field of Search 438/613, 118, 438/612, 615

[56] **References Cited**

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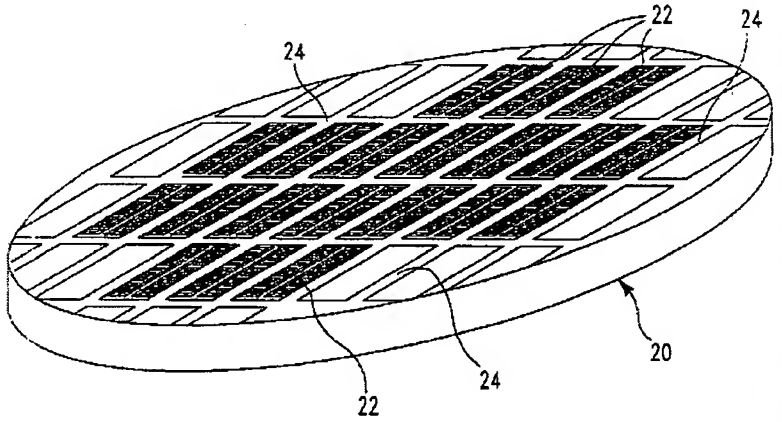
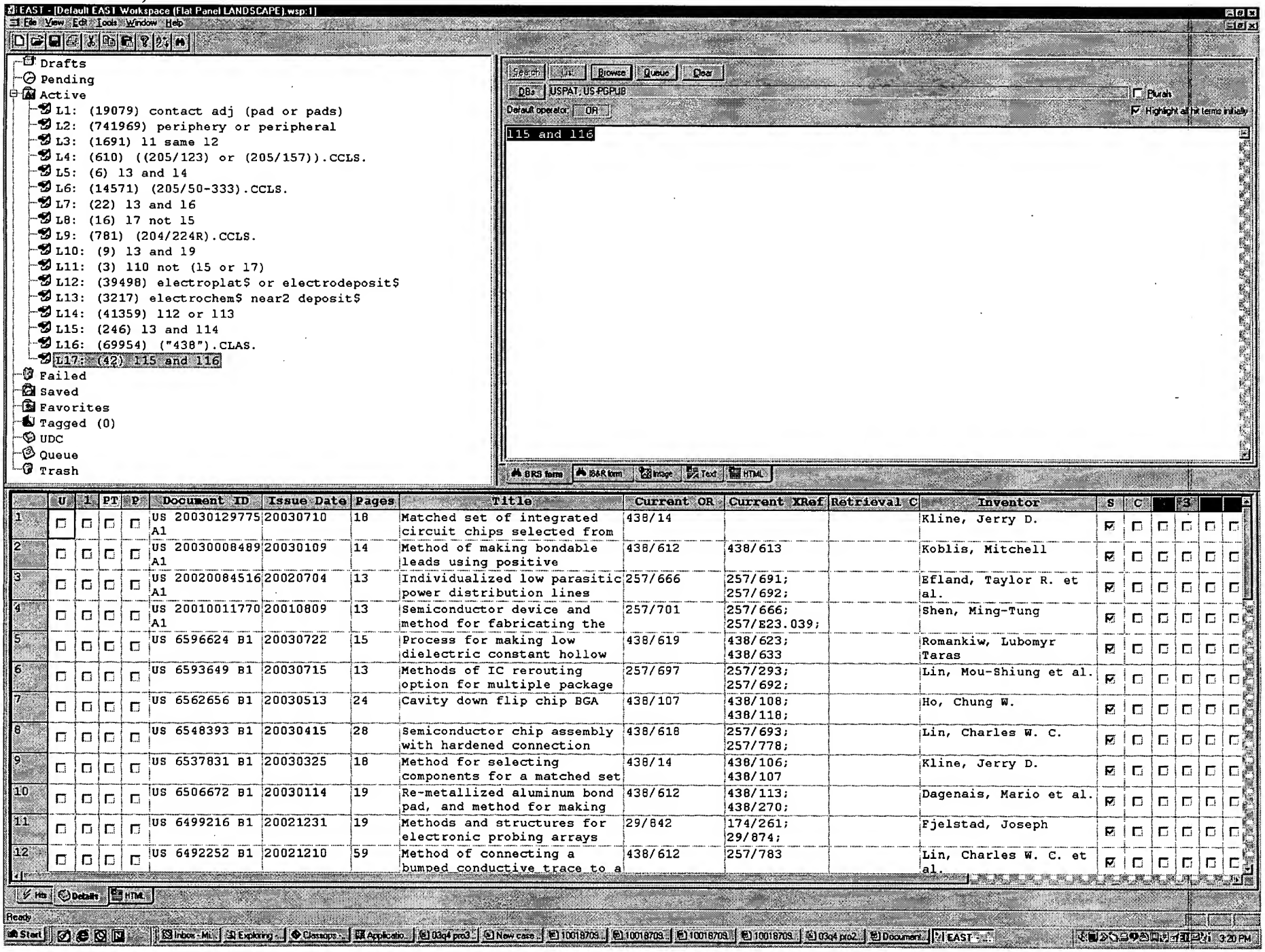
Primary Examiner—Kevin M. Picardat
Assistant Examiner—Deven Collins
Attorney, Agent, or Firm—Robert A. Walsh, Esq.

[57] **ABSTRACT**

Disclosed is a semiconductor wafer, and the method of making the same, the wafer being formed to have a multiplicity of raised contact pads on its surface. The contact pads are formed with conductors which are disposed on the surface of the wafer and which are coupled to internal circuitry embedded in the wafer rough vias in the wafers surface. The contact pads are in a raised elevational relationship relative to the surface conductors. After the wafer is fully processed, by dicing individual integrated circuit chips out of the wafer, each chip can then be mounted on a higher level of assembly, such as a printed circuit board. The raised contact pads originally formed on the wafer, and therefore formed on each individual chip, provide the contact points by which the chip can be bonded with matingly arranged contact pads on the higher level of assembly.

3 Claims, 4 Drawing Sheets





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2	☐	☐	☐	☐	US 20030008489 A1	20030109	14	Method of making bondable leads using positive	438/612	438/613		Koblis, Mitchell	☑	☐	☐
3	☐	☐	☐	☐	US 20020084516 A1	20020704	13	Individualized low parasitic power distribution lines	257/666	257/691; 257/692;		Efland, Taylor R. et al.	☑	☐	☐
4	☐	☐	☐	☐	US 20010011770 A1	20010809	13	Semiconductor device and method for fabricating the	257/701	257/666; 257/E23.039;		Shen, Ming-Tung	☑	☐	☐
5	☐	☐	☐	☐	US 6596624 B1	20030722	15	Process for making low dielectric constant hollow	438/619	438/623; 438/633		Romankiw, Lubomyr Taras	☑	☐	☐
6	☐	☐	☐	☐	US 6593649 B1	20030715	13	Methods of IC rerouting option for multiple package	257/697	257/293; 257/692;		Lin, Mou-Shiung et al.	☑	☐	☐
7	☐	☐	☐	☐	US 6562656 B1	20030513	24	Cavity down flip chip BGA	438/107	438/108; 438/118;		Ho, Chung W.	☑	☐	☐
8	☐	☐	☐	☐	US 6548393 B1	20030415	28	Semiconductor chip assembly with hardened connection	438/618	257/693; 257/778;		Lin, Charles W. C.	☑	☐	☐
9	☐	☐	☐	☐	US 6537831 B1	20030325	18	Method for selecting components for a matched set	438/14	438/106; 438/107		Kline, Jerry D.	☑	☐	☐
10	☐	☐	☐	☐	US 6506672 B1	20030114	19	Re-metallized aluminum bond pad, and method for making	438/612	438/113; 438/270;		Dagenais, Mario et al.	☑	☐	☐
11	☐	☐	☐	☐	US 6499216 B1	20021231	19	Methods and structures for electronic probing arrays	29/842	174/261; 29/874;		Fjelstad, Joseph	☑	☐	☐
12	☐	☐	☐	☐	US 6492252 B1	20021210	59	Method of connecting a bumped conductive trace to a	438/612	257/783		Lin, Charles W. C. et al.	☑	☐	☐

EAST Browser - LG: [20] 4 and 5 | US 6319387 B1 | Tag: 5 | Doc: 4/20 (SORTED) | Format : KWIC

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2	US 6596149 B2	9									USPAT
3	US 6565729 B2	53									USPAT
4	US 6319387 B1	17									USPAT
5	US 6262426 B1	30									USPAT
6	US 6197181 B1	20									USPAT
7	US 6132587 A	12									USPAT

US-PAT-NO: 6319387

DOCUMENT-IDENTIFIER: US 6319387 B1

TITLE: Copper alloy electroplating bath for microelectronic applications

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Brief Summary Text - BSTX (7):
In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path, and I.sub.SAT and V.sub.SAT are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, .rho., of the conductor material. The path capacitance is proportional to the relative dielectric permittivity, K.sub.e, of the dielectric material. A small value of .tau. requires that the interconnect line carry a current density sufficiently large to make the ratio V.sub.SAT/ /RI.sub.SAT small. It follows, therefore, that a low-.rho. conductor that can carry a high current density and a low-K.sub.e dielectric should be utilized in the manufacture of high-performance integrated circuits.

Current US Cross Reference Classification - CCXR (2):
205/123

(12) **United States Patent**
Krishnamoorthy et al.

(10) **Patent No.: US 6,319,387 B1**
(45) **Date of Patent: Nov. 20, 2001**

(54) **COPPER ALLOY ELECTROPLATING BATH FOR MICROELECTRONIC APPLICATIONS**

(75) Inventors: **Ahila Krishnamoorthy**, Menands; **David J. Duquette**, Loudonville; **Shyam P. Murarka**, Clifton Park, all of NY (US)

(73) Assignee: **Semitool, Inc.**, Kalispell, MT (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/386,772**

(22) Filed: **Aug. 31, 1999**

Related U.S. Application Data

(63) Continuation of application No. PCT/US99/14939, filed on Jun. 30, 1999.
(60) Provisional application No. 60/091,691, filed on Jun. 30, 1998, and provisional application No. 60/114,512, filed on Dec. 31, 1998.

(51) **Int. Cl.**[7] **C25D 3/58**
(52) **U.S. Cl.** **205/240**; 205/106; 205/123; 205/239
(58) **Field of Search** 205/239, 240, 205/241, 242, 104, 123; 106/1.23, 1.26

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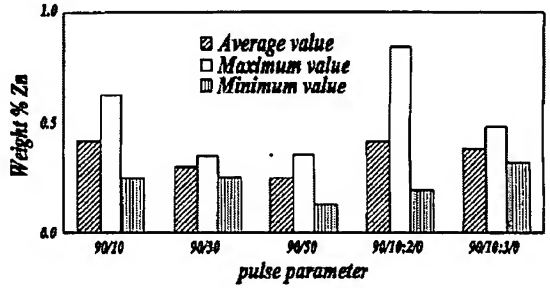
Primary Examiner—Kathryn Gorgos
Assistant Examiner—William T. Leader
(74) *Attorney, Agent, or Firm*—Christensen O'Connor Johnson Kindness PLLC

(57) **ABSTRACT**

A metallized structure for use in a microelectronic circuit is set forth. The metallized structure comprises a dielectric layer, an ultra-thin film bonding layer disposed exterior to the dielectric layer, and a low-Me concentration, copper-Me alloy layer disposed exterior to the ultra-thin film bonding layer. The Me is a metal other than copper and, preferably, is zinc. The concentration of the Me is less than about 5 atomic percent, preferably less than about 2 atomic percent, and even more preferably, less than about 1 atomic percent. In a preferred embodiment of the metallized structure, the dielectric layer, ultra-thin film bonding layer and the copper-Me alloy layer are all disposed immediately adjacent one another. If desired, a primary conductor, such as a film of copper, may be formed exterior to the foregoing layer sequence. The present invention also contemplates methods for forming the foregoing structure as well as electroplating baths that may be used to deposit the copper-Me alloy layer.

12 Claims, 10 Drawing Sheets



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3	US 6565729 B2	53									USPAT
4	US 6319387 B1	17									USPAT
5	US 6262426 B1	30									USPAT
6	US 6197181 B1	20									USPAT
7	US 6132587 A	12									USPAT

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TITLE: Method for electrochemically depositing metal on a semiconductor workpiece

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Brief Summary Text - BSTX (9):

In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path and I.sub.SAT and V.sub.SAT are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, .rho., of the conductor material. The path capacitance is proportional to the relative dielectric permittivity, K.sub.e, of the dielectric material. A small value of .tau. requires that the interconnect line carry a current density sufficiently large to make the ratio V.sub.SAT/ /RI.sub.SAT small. It follows therefore, that a low-.rho. conductor which can carry a high current density and a low-K.sub.e dielectric must be utilized in the manufacture of high-performance integrated circuits.

Current US Cross Reference Classification - CCXR (2):

205/123

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(54) **METHOD FOR ELECTROCHEMICALLY DEPOSITING METAL ON A SEMICONDUCTOR WORKPIECE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/732,513**

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Related U.S. Application Data

(63) Continuation of application No. 09/387,099, filed on Aug. 31, 1999, now Pat. No. 6,277,263, which is a continuation of application No. PCT/US99/06306, filed on Mar. 22, 1999, which is a continuation-in-part of application No. 09/045,245, filed on Mar. 20, 1998, now Pat. No. 6,197,181, and a continuation of application No. PCT/US00/10120, filed on Apr. 13, 2000

(60) Provisional application No. 60/085,675, filed on May 15, 1998, provisional application No. 60/182,160, filed on Feb. 14, 2000, provisional application No. 60/143,769, filed on Jul. 12, 1999, provisional application No. 60/129,055, filed on Apr. 13, 1999, and provisional application No. 60/206,663, filed on May 24, 2000.

(51) **Int. Cl.**[7] **C25D 21/12**

(52) **U.S. Cl.** **205/82**; 205/96; 205/97; 205/123; 205/133; 204/DIG. 7; 427/255.18; 427/255.22; 427/430.1; 427/443.1; 438/758

(58) **Field of Search** ..... 427/255.18, 255.22, 427/430.1, 443.1; 438/758; 204/224 R, 272, 670, DIG. 7; 205/96, 97, 123, 133, 82

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(57) **ABSTRACT**

A process for metallization of a workpiece, such as a semiconductor workpiece. In an embodiment, an alkaline electrolytic copper bath is used to electroplate copper onto a seed layer, electroplate copper directly onto a barrier layer material, or enhance an ultra-thin copper seed layer which has been deposited on the barrier layer using a deposition process such as PVD. The resulting copper layer provides an excellent conformal copper coating that fills trenches, vias, and other microstructures in the workpiece. When used for seed layer enhancement, the resulting copper seed layer provide an excellent conformal copper coating that allows the microstructures to be filled with a copper layer having good uniformity using electrochemical deposition techniques. Further, copper layers that are electroplated in the disclosed manner exhibit low sheet resistance and are readily annealed at low temperatures.

59 Claims, 28 Drawing Sheets